

# Reliability Evaluation Report MDG-MCD-RER1913

ASE Kaohsiung (Taiwan) LQFP7x7 32L & 48L and LQFP10x10 64L Bonding Wire procurement flexibility on listed products (PCN12094)

Gen	eral Information		Traceability	
Commercial Product	<i>STM32F303K8T6 STM32F205RET6 STM8L052C6T6</i>	Diffusio	n Plant	<i>TSMC Fab3 TSMC Fab14 RS8F Rousset Singapore SG8E 8"</i>
Product Line	438X66 411X66 764X19	Assemb	ly Plant	: ASEKH – TAIWAN
Product Description	STM32(5V*438) STM32(5W*411) STM8L(5B*764)			
Package	LQ7x7 32L LQ7x7 48L LQ10x10 64L		Reliabi	lity Assessment
Silicon Technology	0.18 TSMC M10 TSMC F9GO2 RSST F9GO2 SG8E	Pass		
Division	: MDG-MCD	Fail		

**Note:** this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).

Version	Date	Author	Function
1.0	24th September 2021	Berengere Routier-Scappucci	MDG-MCD-QA Back end

### **APPROVED BY:**

Function	Location	Name	Date
Division Q&R Responsible	RSST	Pascal NARCHE	27 <sup>th</sup> September 2021
Division Quality Manager	RSST	Gisele SEUBE	27th September 2021



### TABLE OF CONTENTS

1	RELIA	BILITY	/ EVALUATION OVERVIEW	. 3
	1.1	OBJEC	TIVE	. 3
	1.2	Reliab	BILITY STRATEGY	. 4
	1.3	Conci	LUSION	. 4
2	TEST	VEHIC	CLE CHARACTERISTICS	. 5
	2.1	Gener	ALITIES	. 5
	2.2	TRACE	ABILITY	. 5
	2.	2.1	Wafer fab information	5
	2.	2.2	Assembly information	7
	2.	2.3	Reliability testing information	9
3	TEST	s resu	JLTS SUMMARY	. 9
	3.1	LOT IN	FORMATION	. 9
	3.2	TEST P	PLAN AND RESULTS SUMMARY	10
4	APPL	ICABLE		12
5	GLOS	SARY .		12
6	REVIS	SION H		12



### 1 RELIABILITY EVALUATION OVERVIEW

## 1.1 Objective

The aim of this report is to present results of the reliability evaluation for LQFP 7x7 and LQFP 10x10 packages assembled with silver wires and tested at ASEKH Kaohsiung (Taiwan) for STM8L and STM32.

Production Change Notification PCN12094 concerns same line LQFP 7x7 & 10x10 packages for products in silicon technology F9GO2 Rousset & SG8E.

Changes are described in table below:

		Existing Added			Added
		back-end line			back-end line
Assembly site	Amkor ATP	ST Muar	StatsChipPAC	ASE I	Kaohsiung
	(Philippines)	(Malaysia)	Jiangyin	(Т	aiwan)
			JSCC (China)		
Leadframe	Copper Frame	Copper Frame		Copper Frame	
	Ring Ag	Ring Ag &		Ring Ag	
		Pre Plated Frame			
Leadfinishing	Pure Tin (e3)	Pure Tin (e3) &		Pure Tin (e3)	
(1)		Ni Pd Au (e4)			
Resin (2)	Sumitomo	Sumitomo	Sumitomo	Su	mitomo
	G631HQ	G700LS	G631SHQ	G	631SH
Glue	Evertech	Hitachi	Ablestik	Su	mitomo
	AP4200	EN4900	3230	CRM	1076WA
Wire	Gold 0.8mil	Gold 0.8mil &	Gold 0.8mil &	Gold 0.8mil	
		Silver 96.5%	Silver 96.5%		Silver 96.5%
		0.8mil	0.8mil		0.8mil

(1) Lead color and surface finish change depending on leadfinishing.

(2) Package darkness changes depending on molding compound.

Pin1 identifier can change in terms of form and positioning.



## 1.2 Reliability Strategy

LQFP 7x7 & 10x10 packages is already qualified in Gold wires at ASE Kaohsiung.

Test vehicles are described here below:

Product	Package	Process	Assembly plant	Trials
STM32F303K8T6	LQ7x7 32L	0.18 TSMC		1 assembly lot
STM32F205RET6	LQ10x10 64L	M10 TSMC		1 assembly lot
STM8L052C6T6	LQ7x7 48L	F9GO2 RSST	ASERH - TAIWAN	1 assembly lot
STM8L052C6T6	LQ7x7 48L	F9GO2 SG8E		1 assembly lot

Qualification is based on standard STMicroelectronics Corporate Procedures for Quality and Reliability, in full compliancy with the JESD-47 international standard

## 1.3 Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

According to good reliability tests results in line with reliability strategy, the qualification is granted for packages LQFP 7x7 & 10x10 with silver wires assembled at ASEKH TAIWAN.

Refer to Section 3.0 for reliability test results.



### 2 TEST VEHICLE CHARACTERISTICS

## 2.1 Generalities

Package line	Assembly Line Package	Device (RawLine Code)	Diffusion Process	Number of Lots
	LQFP 32 7x7x1.4	I25V*438ZZXZ	0.18EMBF/2P	1
LQFP 64 10x10x1.4	I45W*411ISX3	CMOSM10ULP	1	
LQFP	LQFP 48 7x7x1.4	I75B*764ISXY CMOSFS	CMOSF9-GO2	1
	LQFP 48 7x7x1.4	I75B*764ISX9	CMOSF9-GO2	1

# 2.2 Traceability

## 2.2.1 Wafer fab information

Wafer fab information		
FAB1	438	
Wafer fab name / location	TSMC Fab3	
Wafer diameter	8 inch	
Wafer thickness	$381\pm25\mu m$	
Silicon process technology	0.18 Gen.Emb.Flash logic TSMC	
Number of masks	33	
Die finishing front side (passivation)	HDPox $10kA \pm SPO(1.5kA \pm PESIN.6kA/1.75um)$	
materials/thicknesses	$10F0X + 10KA + 3KO + 1.5KA + FESIN 0KA/1.75\mu m$	
Die finishing back side		
Materials/thicknesses	NAW SIELCON - BACK GRINDING	
	X:3914µm	
Die area (Stepping die size)	Y:3760µm	
	14.72mm <sup>2</sup>	
Die pad size (X,Y)	65µmx70µm	
Sawing street width (X,Y)	80µmx80µm	
	Tin/AlCu/Tin 0.450	
	Tin/AlCu/Tin 0.450	
Metal levels/Materials/Thicknesses (µm)	Tin/AlCu/Tin 0.450	
	Tin/AlCu/Tin 0.450	
	Tin/AlCu/Tin 0.875	



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#### Table 2

Wafer fab information		
FAB2	411	
Wafer fab name / location	TSMC Fab14	
Wafer diameter	12 inch	
Wafer thickness	775 ± 25µm	
Silicon process technology	CMOSM10ULP	
Number of masks	42	
Die finishing front side (passivation)	IISC + NITRIDE/1.9um	
materials/thicknesses		
Die finishing back side	RAW SILICON	
Materials/thicknesses		
	X:4006µm	
Die area (Stepping die size)	Y:3674µm	
	14.72mm <sup>2</sup>	
Die pad size (X,Y)	59µmx123µm	
Sawing street width (X,Y)	80µmx80µm	
	TaN/Ta/CuSeed/Cu 0.220	
	TaN/Ta/CuSeed/Cu 0.280	
	TaN/Ta/CuSeed/Cu 0.280	
Metal levels/Materials/Thicknesses (µm)	TaN/Ta/CuSeed/Cu 0.280	
	TaN/Ta/CuSeed/Cu 0.280	
	Ta/TaN/AlCu 0.730	
	AlCu 1.200	

Wafer fab information		
FAB3	764	
Wafer fab name / location	F9GO2 Rousset	
Wafer diameter	8 inch	
Wafer thickness	$375 \pm 25 \mu m$	
Silicon process technology	CMOSF9	
Number of masks	39	
Die finishing front side (passivation)	LISC + NitLIV (HEP LISC+LIV Nitride)/1.75um	
materials/thicknesses	$0.50 \pm 10100$ (111 $0.50 \pm 0.0$ Mithue)/1.7 spin	
Die finishing back side		
Materials/thicknesses	NAW SIELCON BACK GRINDING	
	X:1738µm	
Die area (Stepping die size)	Y:2876µm	
	4.998mm <sup>2</sup>	
Die pad size (X,Y)	65μmx108μm	
Sawing street width (X,Y)	80µmx80µm	
	TaN/Ta/Cu 0.280	
	TaN/Ta/Cu 0.350	
Metal levels/Materials/Thicknesses (µm)	TaN/Ta/Cu 0.350	
	TaN/Ta/Cu 0.350	
	Ti/AlCu/TxTN 0.900	



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Table 4

Wafer fab information		
FAB3	764	
Wafer fab name / location	F9GO2 Singapore SG8E	
Wafer diameter	8 inch	
Wafer thickness	375 ± 25µm	
Silicon process technology	CMOSF9	
Number of masks	39	
Die finishing front side (passivation)	USC + NitUV (HEP USC+UV Nitride)/1.75um	
materials/thicknesses	030 + Mtov (Hrr $030+0$ Mthue)/1.75µm	
Die finishing back side		
Materials/thicknesses	KAW SILICON - BACK GRINDING	
	X:1738µm	
Die area (Stepping die size)	Y:2876µm	
	4.998mm <sup>2</sup>	
Die pad size (X,Y)	65µmx108µm	
Sawing street width (X,Y)	80µmx80µm	
	TaN/Ta/Cu 0.280	
	TaN/Ta/Cu 0.350	
Metal levels/Materials/Thicknesses (µm)	TaN/Ta/Cu 0.350	
	TaN/Ta/Cu 0.350	
	Ti/AlCu/TxTN 0.900	

## 2.2.2 Assembly information

Assembly Information – Die 438		
Package 1-LQFP 32 7x7x1.4		
Assembly plant name / location	ASEKH- Taiwan	
Pitch	1.0mm	
Die thickness after back-grinding	$375 \pm 25 \mu m$	
Die sawing method	Step cut	
Bill of Material elements		
Lead frame/reference	LF# A24958 DR Pure tin C7025 4.307sq slots	
Lead frame finishing (material/thickness)	Pure tin thickness: tolerance 7 to 20µm	
Die attach material/type(glue/film)/supplier	GLUE SUMITOMO EPOXY CRM 1076WA	
Wire bonding material/diameter	Wire Ag 96.5 0.8mil diam	
Molding compound material/supplier	MOLDING RESIN SUMITOMO EME-G631SH	
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3	



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#### <u>Table 6</u>

Package 2-LQFP 64 10x10x1.4 - Die 411				
Assembly plant name / location	ASEKH- Taiwan			
Pitch	1.0mm			
Die thickness after back-grinding	$375 \pm 25 \mu m$			
Die sawing method	Laser Groove + mechanical sawing			
Bill of Material elements				
Lead frame/reference	LF# A25060 LQ64 Pure Tin C7025 5.7sq			
Lead frame finishing (material/thickness)	Pure tin thickness: tolerance 7 to 20µm			
Die attach material/type(glue/film)/supplier	GLUE SUMITOMO EPOXY CRM 1076WA			
Wire bonding material/diameter	Wire Ag 96.5 0.8mil diam			
Molding compound material/supplier	MOLDING RESIN SUMITOMO EME-G631SH			
Package Moisture Sensitivity Level (JEDEC J–STD020D)	3			

Package 3-LQFP 48 7x7x1.4 - Die 764				
Assembly plant name / location	ASEKH- Taiwan			
Pitch	1.0mm			
Die thickness after back-grinding	$375 \pm 25 \mu m$			
Die sawing method	Step cut			
Bill of Material elements				
Lead frame/reference	LF# A24950 LQ48L Pur tin C7025 4.092sq			
Lead frame finishing (material/thickness)	Pure tin thickness: tolerance 7 to 20µm			
Die attach material/type(glue/film)/supplier	GLUE SUMITOMO EPOXY CRM 1076WA			
Wire bonding material/diameter	Wire Ag 96.5 0.8mil diam			
Molding compound material/supplier	MOLDING RESIN SUMITOMO EME-G631SH			
Package Moisture Sensitivity Level	3			
(JEDEC J–STD020D)	-			



### 2.2.3 Reliability testing information

#### Table 8

Reliability Testing Information	
Reliability laboratory name / location	Rousset/France

<u>Note:</u> ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs. ST certification document can be downloaded under the following link: <u>http://www.st.com/content/st\_com/en/support/guality-and-reliability/certifications.html</u>

### **3 TESTS RESULTS SUMMARY**

## 3.1 Lot Information

Lot #	Diffusion Lot / Wafer ID	Die Revision (Cut)	Assy Lot / Trace Code	Raw Line	Package	Note
1	93929045	Cut 1.1	AA943155	I25V*438ZZXZ	LQFP 32 7x7x1.4	Dackaga
2	9R807141	Cut 2.5	AA942042	I45W*411ISX3	LQFP 64 10x10x1.4	Package
3	VG808155	Cut 2.1	AA939125	I75B*764ISXY	LQFP 48 7x7x1.4	assessment
4	VC907X41	Cut 2.1	AA952169	I75B*764ISX9	LQFP 48 7x7x1.4	assessment



## 3.2 Test plan and results summary

#### Table 10 – ACCELERATED ENVIRONMENT STRESS TESTS

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	250V	4	3	12	Lot1: 0/3 Lot2: 0/3 Lot3: 0/3 Lot4: 0/3	
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	4	308	1232	Lot1: 0/308 Lot2: 0/308 Lot3: 0/308 Lot4: 0/308	
тс	JESD22-A104	Ta=-65/150°C Duration= 500cyc ⊠ After PC	4	77	308	Lot1: 0/77 Lot2: 0/77 Lot3: 0/77 Lot4: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ⊠ After PC	4	77	308	Lot1: 0/77 Lot2: 0/77 Lot3: 0/77 Lot4: 0/77	
HTSL	JESD 22-A103	Ta=150°C , Duration= 1000hrs ⊠ After PC	4	77	308	Lot1: 0/77 Lot2: 0/77 Lot3: 0/77 Lot4: 0/77	
ТНВ	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 Duration= 1000hrs ⊠ After PC	4	77	308	Lot1: 0/77 Lot2: 0/77 Lot3: 0/77 Lot4: 0/77	

Note: Test method revision reference is the one active at the date of reliability trial execution



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#### Table 11 - PACKAGE ASSEMBLY INTEGRITY TESTS

Fail/S.S. (N/A = Not Ap	oplicable)
CA Construction Analysis including -Wire bond shear -Wire bond pull ST Internal specifications 4 4 40 40 40 40 40 40 40 40 40 40 40 40	ROUSSET diff plant)



## **4 APPLICABLE AND REFERENCE DOCUMENTS**

Reference	Short description
ANSI/ESDA JEDEC JS-002	Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
J-STD-020:	Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices
JESD22-A113:	Preconditioning of non-hermetic surface mount devices prior to reliability testing
JESD22-A118:	Unbiased Highly Accelerated temperature & humidity Stress Test
JESD22-A110:	Temperature Humidity Bake
JESD22-A104:	Temperature cycling

### 5 GLOSSARY

Reference	Short description
PC	Preconditioning (solder simulation)
ТНВ	Temperature Humidity Bias
тс	Temperature cycling
uHAST	Unbiased Highly Accelerated Stress Test
HTSL	High temperature storage life
DMS	ST Advanced Documentation Controlled system/ Documentation Management system
ESD CDM	Electrostatic discharge (charge device model)
CA	Construction Analysis

### **6** REVISION HISTORY

Pavision	Author	Content	Approval List				
REVISION		description	Function	Location	Name	Date	
1.0	B Routier- Scappucci	Initial release	Division Q&R	ST Rousset	Gisèle SEUBE	27 <sup>th</sup> September	
			Responsible			2021	
			Division Quality			27 <sup>th</sup> September	
			Manager	STROUSSEL	Fascal NARCHE	2021	



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# PRODUCT/PROCESS CHANGE NOTIFICATION PCN12094– Additional information

# ASE Kaohsiung (Taiwan) LQFP7x7 32L & 48L and LQFP10x10 64L Bonding Wire procurement flexibility On listed products

## MDG - Microcontrollers Division (MCD)

#### What are the changes?

Changes described in table below:

				Existing	Added
				back-end line	back-end line
Assembly site	Amkor ATP	ST Muar	StatsChipPAC	ASE ł	Kaohsiung
	(Philippines)	(Malaysia)	Jiangyin	(Т	aiwan)
			JSCC (China)		
Leadframe	Copper Frame	Copper Frame		Copper Frame	
	Ring Ag	Ring Ag &		Ring Ag	
		Pre Plated Frame			
Leadfinishing	Pure Tin (e3)	Pure Tin (e3) &		Pure Tin (e3)	
(1)		Ni Pd Au (e4)			
Resin (2)	Sumitomo	Sumitomo	Sumitomo Sumitomo		mitomo
	G631HQ	G700LS	G631SHQ	G631SH	
Glue	Evertech	Hitachi	Ablestik	Su	mitomo
	AP4200	EN4900	3230 CRM 1076WA		1076WA
Wire	Gold 0.8mil	Gold 0.8mil &	Gold 0.8mil & Gold 0.8mil		
		Silver 96.5% 0.8mil	Silver 96.5% 0.8mil		Silver 96.5% 0.8mil

(1) Lead color and surface finish change depending on leadfinishing.



(2) Package darkness changes depending on molding compound.

Pin1 identifier can change in terms of form and positioning. Marking position and size could be different upon assembly site, without any loss of information.



#### How to order samples?

- For all samples request linked to this PCN, please:
- place a <u>Non-standard</u> sample order (choose Sample Non Std Type from pull down menu)
- insert the PCN number "PCN12094" into the NPO Electronic Sheet/Regional Sheet
- request sample(s) through Notice tool, indicating a single Commercial Product for each request

	rtial Ship:	01 - Price F	ol: 05 Statu	s: 01 Canc:	-		
	<b>%</b> : 0	Sample Type	: Sample Nor	Std Type	-		
		-	Sample Std	Типе	-		
		Closing Type	Sample Nor	1 Std Type			
			Sample Nor	Stdw Spl Tes	ts		
		Lab She	et:				
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SO   NPO Sample							-07
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Header							1010100000000000000
SO Nr: 8018502433	Customer: 99770200	01 ST-TOKYO	SO Type: 3	0 Sample Order	Cost C	enter: JT3129	SAMPLES /SALE
PO Nr.		Carrier Code: 0001	Price Policy: 05	Currency: 02 4.5	DOLLAR	Reg Name:	
Notes:	Status: 01	All items pending,ni	Issuing Date: 25	JUN-2018 Ord V	t 0.0000	Sample Req D	ate: 25-Jun-2018
Sch I Nr PO I. Nr.	Finished Good	Comm Qty Open Qty	Plant Open Qty	Read Qty Unit Price	RD	CD	EDD S
1.1.10 000001	STM32F429NIH6 3	0 30	30	30 0.0000	25-Jun-18	01-Mar-59	01-Mar-59 0
•							
Final Cust:					1		
PO Item: 000001 Comm	Prodit STM32F429NII	16 Qty: 30	RD: 25-Jun	18 Unit Price:	0.0000 Fina	l Cust 8800367	006 SANSHIN/
Cust Part Nr:	Finishd Go	xt:	Partial Ship	01 - Price Po	t 05 Status	1 Canc:	
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Project Name:		Closin	g Date:	Closing Type:		*	
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